ACADEMIC REGULATIONS
COURSE STRUCTURE &
DETAILED SYLLABI

M. Tech Regular Two Year Degree Courses
(For the Batches Admitted From 2012-2013)

POWER ELECTRONICS AND ELECTRICAL DRIVES (PE & ED)

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY
(AUTONOMOUS)
R.V.S. Nagar, CHITTOOR – 517 127, A.P
Phones: (08572) 246339, 245044 Fax: (08572) – 245211
The Jawaharlal Nehru Technological University Anantapur shall confer M.Tech Post Graduate degree to candidates who are admitted to the Master of Technology Programs and fulfill all the requirements for the award of the degree.

**1.0 ELIGIBILITY FOR ADMISSIONS:**

Admission to the above programme shall be made subject to the eligibility, qualifications and specialization prescribed by the competent authority for each programme, from time to time.

Admissions shall be made either on the basis of merit rank obtained by the qualified candidates at an Entrance Test conducted by the University or on the basis of GATE/PGECET score, subject to reservations and policies prescribed by the Government from time to time.

**2.0 ADMISSION PROCEDURE:**

As per the existing stipulations of AP State Council for Higher Education (APSCHE), Government of Andhra Pradesh, admissions are made into the first year as follows:

a) Category –A seats are to be filled by Convenor through PGECET/GATE score.
b) Category-B seats are to be filled by Management as per the norms stipulated by Government of A.P.

**3.0 Specializations:**

<table>
<thead>
<tr>
<th>Sl. No</th>
<th>Department</th>
<th>Specializations</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>CSE</td>
<td>Computer Science &amp; Engg.</td>
</tr>
<tr>
<td>2.</td>
<td>CSE</td>
<td>Computer Science</td>
</tr>
<tr>
<td>3.</td>
<td>EEE</td>
<td>Power Electronics &amp; Electrical Drives</td>
</tr>
<tr>
<td>4.</td>
<td>ECE</td>
<td>VLSI System Design</td>
</tr>
<tr>
<td>5.</td>
<td>ECE</td>
<td>Digital Electronics and Communication System</td>
</tr>
<tr>
<td>6.</td>
<td>ECE</td>
<td>Embedded systems</td>
</tr>
<tr>
<td>7.</td>
<td>IT</td>
<td>Software Engg.</td>
</tr>
<tr>
<td>8.</td>
<td>ME</td>
<td>CAD/CAM</td>
</tr>
<tr>
<td>9.</td>
<td>CE</td>
<td>Structural Engg.</td>
</tr>
</tbody>
</table>
4.0 COURSE WORK:
4.1. A Candidate after securing admission must pursue the M.Tech course of study for Four Semesters duration.
4.2. Each semester shall have a minimum of 16 instructional weeks.
4.3. A candidate admitted to a programme should complete it within a period equal to twice the prescribed duration of the programme from the date of admission.

5.0 ATTENDANCE:
5.1. A candidate shall be deemed to have eligibility to write end semester examinations if he has put in at least 75% of attendance on cumulative basis of all subjects/courses in the semester.
5.2. Condonation of shortage of attendance up to 10% i.e., from 65% and above and less than 75% may be given by the college on the recommendation of the Principal.
5.3. Condonation of shortage of attendance shall be granted only on medical grounds and on representation by the candidate with supporting evidence.
5.4. If the candidate does not satisfy the attendance requirement he is detained for want of attendance and shall reregister for that semester. He shall not be promoted to the next semester.

6.0 EVALUATION:
The performance of the candidate in each semester shall be evaluated subject wise, with a maximum of 100 marks for Theory and 100 marks for practicals, on the basis of Internal Evaluation and End Semester Examination.
6.1. For the theory subjects 60% of the marks will be for the External End Examination. While 40% of the marks will be for Internal Evaluation, based on the better of the marks secured in the two Mid Term-Examinations held, one in the middle of the Semester (I-IV units) and another immediately after the completion of instruction (V-VIII units) with four questions to be answered out of five in 2 hours, evaluated for 40 marks.
6.2. For practical subjects, 60 marks shall be for the End Semester Examinations and 40 marks will be for internal evaluation based on the day to day performance (25 marks) and practical test at the end of the semester (15 marks).
6.3. For Seminar there will be an internal evaluation of 50 marks. A candidate has to secure a minimum of 50% to be declared successful. The assessment will be made by a board consisting of HOD and two internal experts.
6.4. A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.
6.5. In case the candidate does not secure the minimum academic requirement in any of the subjects (as specified in 6.4) he has to reappear for the Semester Examination either supplementary or regular in that subject, or repeat the subject when next offered or do any other specified subject as may be required.

6.6. **Revaluation / Recounting:**

Students shall be permitted for request for recounting/revaluation of the year / Semester-End examination answer scripts within a stipulated period after payment of prescribed fee. After recounting or revaluation, records are updated with changes if any and the student will be issued a revised grade sheet. If there are no changes, the same will be intimated to the students.

6.7 **Supplementary Examination:**

In addition to the regular year/ Semester- End examinations conducted, the College may also schedule and conduct supplementary examinations for all the subjects of other year/ semesters when feasible for the benefit of students. Such of the candidates writing supplementary examinations may have to write more than one examination per day.

7.0 **RE-REGISTRATION:**

Following are the conditions to avail the benefit of improvement of internal evaluation marks

7.1. The candidate should have completed the course work and obtained examinations results for I & II semesters.

7.2. He should have passed all the subjects for which the internal evaluation marks secured are more than or equal to 50%.

7.3. Out of the subjects the candidate has failed in the examination due to internal evaluation marks secured being less than 50%, the candidate shall be given one chance for each Theory subject and for a maximum of three Theory subjects for Improvement of Internal evaluation marks.

7.4. The candidate has to re-register for the chosen subjects and fulfill the academic requirements.

7.5. For each subject, the candidate has to pay a fee equivalent to one third of the semester tuition fee and the along with the requisition to the Principal of the college.

7.6. In the event of availing the Improvement of Internal evaluation marks, the internal evaluation marks as well as the End Examinations marks secured in the previous attempt(s) for the reregistered subjects stand cancelled.
8.0 EVALUATION OF PROJECT WORK:

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the department.

8.1. Registration of Project work: A candidate is permitted to register for the project work after satisfying the attendance requirement of I & II Semesters.

8.2. An Internal Departmental Committee (I.D.C) consisting of HOD, Supervisor and one internal senior teacher shall monitor the progress of the project work.

8.3. The work on the project shall be initiated in the penultimate semester and continued in the final semester. The duration of the project is for two semesters. The candidate can submit Project thesis with the approval of I.D.C. after 36 weeks from the date of registration at the earliest. Extension of time within the total permissible limit for completing the programme is to be obtained from the Head of the Institution.

8.4. The student must submit status report at least in three different phases during the project work period. These reports must be approved by the I.D.C before submission of the Project Report and award internal assessment marks for 120.

8.5. A candidate shall be allowed to submit the Thesis / Dissertation only after passing in all the prescribed subjects (both theory and practical) and then take viva voce examination of the project. The viva voce examination may be conducted once in two months for all the candidates who have submitted thesis during that period.

8.6. Three copies of the Thesis / Dissertation certified in the prescribed form by the supervisor and HOD shall be presented to the HOD. One copy is to be forwarded to the Controller of Examinations and one copy to be sent to the examiner.

8.7. The Dept shall submit a panel of three experts for a maximum of 5 students at a time. However, the Thesis / Dissertation will be adjudicated by one examiner nominated by the Chief Controller Of Examinations.

8.8. If the report of the examiner is favorable viva-voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the thesis / dissertation. The board shall jointly award the marks for 180.

8.9. A candidate shall be deemed to have secured the minimum academic requirement in the project work if he secures a minimum of 50% marks in the viva-voce examination and a minimum aggregate of 50% of the total marks in the end viva-voce examination and the internal project report taken together. If he fails to get the minimum academic requirement he has to appear for the viva-voce examination again to get the minimum marks.
If he fails to get the minimum marks at the second viva-voce examination he will not be eligible for the award of the degree, unless the candidate is asked to revise and resubmit. If the candidate fails to secure minimum marks again, the project shall be summarily rejected.

9.0 **Grades, Grade point Average, Cumulative Grade point Average:**

9.1. **Grade System:** After all the components and sub-components of any subject (including laboratory subjects) are evaluated, the final total marks obtained will be converted to letter grades on a “10 point scale” described below.

<table>
<thead>
<tr>
<th>% of marks obtained</th>
<th>Grade</th>
<th>Grade Points(GP)</th>
</tr>
</thead>
<tbody>
<tr>
<td>90 to 100</td>
<td>A+</td>
<td>10</td>
</tr>
<tr>
<td>80 to 89</td>
<td>A</td>
<td>9</td>
</tr>
<tr>
<td>70 to 79</td>
<td>B</td>
<td>8</td>
</tr>
<tr>
<td>60 to 69</td>
<td>C</td>
<td>7</td>
</tr>
<tr>
<td>50 to 59</td>
<td>D</td>
<td>6</td>
</tr>
<tr>
<td>Less than 50 in sum of Int. and Ext. (or) Less than 24 in Ext.</td>
<td>F</td>
<td>0</td>
</tr>
<tr>
<td>Not Appeared</td>
<td>N</td>
<td>0</td>
</tr>
</tbody>
</table>

9.2. **GPA:** Grade Point Average (GPA) will be calculated as given below on a “10 Point scale” as an Index of the student’s performance at the end of each semester:

$$GPA = \frac{\sum(C \times GP)}{\sum C}$$

Where C denotes the credits assigned to the subjects undertaken in that semester and GP denotes the grade points earned by the student in the respective subjects.

9.3. **CGPA:** At the end of every semester, a Cumulative Grade Point Average (CGPA) on a 10 Point scale is computed considering all the subjects passed up to that point as an index of overall Performance up to that Point as given below:

$$CGPA = \frac{\sum(C \times GP)}{\sum C}$$

Where C denotes the credits assigned to subjects undertaken upto the end of the current semester and GP denotes the grade points earned by the student in the respective courses.

9.4. **Grade sheet:** A grade sheet (Marks Memorandum) will be issued to each student indicating his performance in all subjects registered in that semester indicating the GPA and CGPA. GPA and CGPA will be rounded off to the second place of decimal.

9.5 **Transcripts:** After successful completion of the entire Program of study, a transcript containing performance of all semesters will be issued as a final record. Duplicate transcripts will also be issued, if required, after payment of requisite fee.
10.0 **Award of Degree:** The Degree will be conferred and awarded by Jawaharlal Nehru Technological University Anantapur, Anantapur on the recommendation of The Principal of SVCET (Autonomous).

10.1 **Eligibility:** A student shall be eligible for the award of M.Tech. Degree if he fulfills all the following conditions:

- Registered and successfully completed all the components prescribed in the program of study for which he is admitted.
- Successfully acquired the minimum required credits as specified in the curriculum corresponding to the specialization of study within the stipulated time.
- Obtained CGPA greater than or equal to 6.0 (Minimum requirement for declaring as passed.)

10.1 **Award of Class:** Declaration of Class is based on CGPA.

<table>
<thead>
<tr>
<th>Cumulative Grade Point Average</th>
<th>Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>≥7.0</td>
<td>First Class with Distinction</td>
</tr>
<tr>
<td>&gt;6.0 and &lt;7.0</td>
<td>First Class</td>
</tr>
<tr>
<td>6.0</td>
<td>Second Class</td>
</tr>
</tbody>
</table>

11.0 **WITH – HOLDING OF RESULTS:** If the candidate has not paid dues to the university/college or if any case of in-discipline is pending against him, the result of the candidate shall be withheld and he will not be allowed/promoted into the next higher semester. The issue of degree is liable to be withheld in such cases.

12.0 **TRANSITORY REGULATIONS:** Candidates who have discontinued or have been detained for want of attendance or who have failed after having undergone the course in earlier regulations and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same or equivalent subjects as and when subjects are offered, subject to 6.5 and 4.3 sections. Whereas they continue to be in the academic regulations of the batch they join later.

13.0 **GENERAL:**

i. The academic regulations should be read as a whole for purpose of any interpretation.

ii. Disciplinary action for Malpractice/improper conduct in examinations is appended.

iii. Where the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”, “hers”.

iv. In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Principal is final.

v. The college may change or amend the academic regulations or syllabi at any time and the changes or amendments shall be made applicable to all the students on rolls with effect from the dates notified by the college.

*****
Identification of Courses

M. Tech

Each course shall be uniquely identified by an alphanumeric code of width 7 characters as given below.

<table>
<thead>
<tr>
<th>No. of digits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>First two digits</td>
<td>Year of regulations Ex: 12</td>
</tr>
<tr>
<td>Next one letter</td>
<td>Type of program: A: B. Tech</td>
</tr>
<tr>
<td></td>
<td>B: M. Tech</td>
</tr>
<tr>
<td></td>
<td>C: M.B.A</td>
</tr>
<tr>
<td></td>
<td>D: M.C.A</td>
</tr>
<tr>
<td>Next two letters</td>
<td>Code of program: P.E: Power Electronics &amp; Electric Drives, VL: VLSI,</td>
</tr>
<tr>
<td></td>
<td>DE: DECS, EM: Embedded Systems, CM: CAD/CAM, CS: Computer Science and</td>
</tr>
<tr>
<td></td>
<td>Engineering</td>
</tr>
<tr>
<td>Last two digits</td>
<td>Indicate serial numbers: ≥ 01</td>
</tr>
</tbody>
</table>

Ex:
12BST01
12BPE01
12BVL01
12BDE01
12BEM01
12BCM01
12BCS01
12BSE01
12BCO01
**RULES FOR DISCIPLINARY ACTION FOR MALPRACTICE / IMPROPER CONDUCT IN EXAMINATIONS**

<table>
<thead>
<tr>
<th>Nature of Malpractices / Improper conduct</th>
<th>Punishment</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>If the candidate</strong></td>
<td></td>
</tr>
<tr>
<td>1. (a) Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)</td>
<td>Expulsion from the examination hall and cancellation of the performance in that subject only.</td>
</tr>
<tr>
<td>(b) Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.</td>
<td>Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.</td>
</tr>
<tr>
<td>2. Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.</td>
<td>Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled.</td>
</tr>
<tr>
<td></td>
<td>3.</td>
</tr>
<tr>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td></td>
<td>4.</td>
</tr>
<tr>
<td></td>
<td>5.</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>6.</td>
<td>Possess any lethal weapon or firearm in the examination hall.</td>
</tr>
<tr>
<td>7.</td>
<td>Impersonates any other candidate in connection with the examination.</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td><strong>8.</strong></td>
<td>Refuses to obey the orders of the Chief Superintendent / Assistant – Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in-charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.</td>
</tr>
<tr>
<td><strong>9.</strong></td>
<td>If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.</td>
</tr>
<tr>
<td></td>
<td>Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.</td>
</tr>
<tr>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>10.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.</th>
<th>Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.</th>
</tr>
</thead>
<tbody>
<tr>
<td>11.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the Examination committee for further action to award suitable punishment.</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>12.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Malpractices identified by squad or special invigilators

1. Punishments to the candidates as per the above guidelines.
## I M.Tech, I Semester

<table>
<thead>
<tr>
<th>S.No</th>
<th>Code</th>
<th>Subject</th>
<th>Periods</th>
<th>Credits</th>
<th>Scheme of Examination (Maximum Marks)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>T</td>
<td>P</td>
</tr>
<tr>
<td>1</td>
<td>12BPE01</td>
<td>Advanced Power Semiconductor Devices and Protection</td>
<td>4</td>
<td>1</td>
<td>-</td>
</tr>
<tr>
<td>2</td>
<td>12BPE02</td>
<td>Analysis of Power Converters</td>
<td>4</td>
<td>1</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>12BPE03</td>
<td>Power Electronic Control of DC Drives</td>
<td>4</td>
<td>1</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>12BPE04</td>
<td>Principles of Machine modeling and Analysis</td>
<td>4</td>
<td>1</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Elective – I</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>12BPE05</td>
<td>DSP Applications in Electrical Engineering</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>12BPE06</td>
<td>Digital Control Systems</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>12BPE07</td>
<td>Computer Aided Design of Electrical Machines</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Elective – II</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>12BPE08</td>
<td>PIC Controllers and Applications</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>12BPE09</td>
<td>Computer Aided Design of Power Electronics Circuits</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>12BPE10</td>
<td>Advanced Power System Operation &amp; Control</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>12BPE11</td>
<td>Simulation of Power Electronic Systems Lab</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>12BPE12</td>
<td>D.C Drives lab</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>12BPE13</td>
<td>Seminar -I</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Total**

<table>
<thead>
<tr>
<th>L</th>
<th>T</th>
<th>P</th>
<th>Internal</th>
<th>External</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>24</td>
<td>6</td>
<td>4</td>
<td>28</td>
<td>370</td>
<td>480</td>
</tr>
</tbody>
</table>

## I M.Tech, II Semester

<table>
<thead>
<tr>
<th>S.No</th>
<th>Code</th>
<th>Subject</th>
<th>Periods</th>
<th>Credits</th>
<th>Scheme of Examination (Maximum Marks)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>T</td>
<td>P</td>
</tr>
<tr>
<td>1</td>
<td>12BPE14</td>
<td>Analysis of Inverters</td>
<td>4</td>
<td>1</td>
<td>-</td>
</tr>
<tr>
<td>2</td>
<td>12BPE15</td>
<td>Power Electronic Control of AC Drives</td>
<td>4</td>
<td>1</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>12BPE16</td>
<td>Power Electronics for Renewable Energy Sources</td>
<td>4</td>
<td>1</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>12BPE17</td>
<td>Power Electronics Applications in Power Systems</td>
<td>4</td>
<td>1</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Elective – III</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>12BPE18</td>
<td>Embedded System Design</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>12BPE19</td>
<td>Intelligent Control of Electrical Drives</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>12BPE20</td>
<td>Modern Rectifiers and Resonant Converters</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Elective – IV</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>12BPE21</td>
<td>Optimal Control Theory</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>12BPE22</td>
<td>System Identification and Adaptive Control</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>12BPE23</td>
<td>Electrical Distribution and Automation.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>12BPE24</td>
<td>A.C. Drives lab</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>12BPE25</td>
<td>Embedded Systems Lab</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>12BPE26</td>
<td>Seminar -II</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>12BPE27</td>
<td>Comprehensive viva voce</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Total**

<table>
<thead>
<tr>
<th>L</th>
<th>T</th>
<th>P</th>
<th>Internal</th>
<th>External</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>24</td>
<td>6</td>
<td>4</td>
<td>30</td>
<td>470</td>
<td>480</td>
</tr>
</tbody>
</table>
### II M.Tech, III & IV Semester

<table>
<thead>
<tr>
<th>S.No</th>
<th>Code</th>
<th>Subject</th>
<th>Periods</th>
<th>Credits</th>
<th>Scheme of Examination (Maximum Marks)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>T</td>
<td>P</td>
</tr>
<tr>
<td>1</td>
<td>12BPE28</td>
<td>Project Work</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Department of Electrical and Electronics Engineering
UNIT I : BJTS:
Introduction- vertical power transistor structures-I-V characteristics-physics of BJT operation switching characteristics-break down voltages-second break down-on-state losses-safe operation areas design of drive circuits for BJTs-snubber circuits for BJTs and darlington.

UNIT II : POWER MOSFETS:
Introduction-basic structures-I-V characteristics-physics of device operation-switching characteristics-operation limitations and safe operating areas-design of gate drive circuits-snubber circuits.

UNIT III : GATE TURN-OFF THYRISTORS:
Introduction-basic structures-I-V characteristics-physics of device operation-GTO switching characteristics-snubber circuits-over protection of GTOs.

UNIT IV : INSULATED GATE BIPOLAR TRANSISTORS:
Introduction-basic structures-I-V characteristics-physics of device operation-Latch in IGBTs-switching characteristics-Device limits and safe operating areas-drive and snubber circuits.

UNIT V : EMERGING DEVICES AND CIRCUITS:
Introduction-Power junction field effect transistors-field controlled Thyristor-JFET based devices versus other power devices-MOS controlled Thyristors-high voltage integrated circuits-new semiconductor materials.

UNIT VI : PASSIVE COMPONENTS AND ELECTROMAGNETIC COMPATIBILITY:
Introduction-design of inductor-transformer design-selection of capacitors-resistors current measurements-heat sinking circuit lay out –Electromagnetic Interference (EMI)-Sources of EMI-Electromagnetic Interference in Power Electronic Equipment

UNIT VII : NOISE:
Noise sources in SMPS-Diode Storage Charge Noise-Noise generated due to switching-Common noises sources in SMPS-Noises Due to High frequency transformer-How the conducted noise is measured - minimizing EMI-EMI shielding-EMI standards.

UNIT VIII : PROTECTION OF DEVICES & CIRCUITS:

TEXT BOOKS:
1. Power Electronics –Converters, Applications and Design – Mohan and Undeland-John Wiley&Sons
2. Power Electronics Circuits, Devices and Applications – M.H.Rashid-PHI-Publication

REFERENCE BOOKS:
1. Power Electronics Circuits-Vithayathil
2. Power Electronics Circuits-W.C. Lander
UNIT I: STATIC AND DYNAMIC CHARACTERISTICS:
Static and Dynamic Characteristics of power diode, SCR, MOSFET, IGBT and GTO-
Series and parallel operation - Protection circuits - Numerical Problems

UNIT II: SINGLE PHASE AC-DC CONVERTER:
Single phase - Half controlled and fully controlled Converters - Evaluation of input
power factor and harmonic factor - Continuous and Discontinuous load current - Single phase
dual converters - Power factor improvements - Extinction angle control - symmetrical angle
control - PWM single phase sinusoidal PWM - Single phase series converters -- Application-
umerical problems

UNIT III: THREE PHASE AC-DC CONVERTER:
Three Phase Converters - Half controlled and fully controlled Converters - Evaluation
of input power factor and harmonic factor - Continuous and Discontinuous load current-
Application - numerical problems

UNIT IV: D.C. TO D.C CONVERTERS:
Principle and operation of step down chopper condition of duty cycle - step down
converter with R load - Performance parameter Analysis of step-down and step up dc to dc
converters with resistive and resistive - inductive loads

UNIT V: D.C. TO D.C CONVERTERS:
Analysis of Switched mode regulators - Analysis of Buck regulators - Boost Regulators-
Buck-Boost Regulators - Cuk Regulators - Condition for continuous inductor and capacitor
voltage - Comparison of regulators - Multi output boost regulators - advantages - Application-
umerical problems

UNIT VI: SINGLE PHASE AC VOLTAGE CONTROLLERS:
Single Phase AC Voltage Controllers with resistive, resistive-inductive and resistive-
inductive-induced emf loads - ac voltage controller's wit PWM control - Effects of source and
load inductances - asynchronous tap changers - Application - numerical problems

UNIT VII: THREE PHASE AC VOLTAGE CONTROLLERS:
Three Phase AC Voltage controllers - Analysis of Controllers with star and delta
connected resistive, resistive - inductive loads - Effects of source and load inductances-
Application - numerical problems.

UNIT VIII: DUAL CONVERTERS & CYCLOCONVERTERS:
Single phase & three phase dual converters - Power factor improvements - three phase
PWM-twelve pulse converters - Application - numerical problems - Single phase to single
phase cycloconverters - analysis of midpoint and bridge configurations - three phase to three
phase cycloconverters - analysis of Midpoint and bridge configurations - Limitations-
Advantages - Applications - numerical problems

TEXT BOOKS:
1. Rashid M.H, 'Power Electronics – Circuits, Devices & Applications”, Prentice Hall of India,
REFERENCE BOOKS:
UNIT I: CONTROLLED BRIDGE RECTIFIER (1-Ф) WITH DC MOTOR LOAD:
Separately excited DC motors with rectified single phase supply - single phase semi converter and single phase full converter for continuous and discontinuous modes of operation – power and power factor.

UNIT II: CONTROLLED BRIDGE RECTIFIER (3-Ф) WITH DC MOTOR LOAD:
Three phase semi converter and three phase full converter for continuous and discontinuous modes of operation – power and power factor – Addition of Freewheeling diode – Three phase double converter.

UNIT III: THREE PHASE NATURALLY COMMUTATED BRIDGE CIRCUIT AS A RECTIFIER OR AS AN INVERTER:
Three phase controlled bridge rectifier with passive load impedance, resistive load and ideal supply – Highly inductive load and ideal supply for load side and supply side quantities, shunt capacitor compensation, three phase controlled bridge rectifier inverter.

UNIT IV: PHASE CONTROLLED DC MOTOR DRIVES:

UNIT V: CURRENT AND SPEED CONTROLLED DC MOTOR DRIVES:

UNIT VI: CHOPPER CONTROLLED DC MOTOR DRIVES:

UNIT VII: CLOSED LOOP OPERATION OF DC MOTOR DRIVES:
Speed controlled drive system – current control loop – pulse width modulated current controller – hysteresis current controller – modeling of current controller – design of current

UNIT VIII: SIMULATION OF DC MOTOR DRIVES:
Dynamic simulations of the speed controlled DC motor drives – Speed feedback speed controller – command current generator – current controller.

TEXT BOOKS:

REFERENCES:
UNIT I: BASIC CONCEPTS OF MODELING:
Basic Two-pole Machine representation of Commutator machines, 3-phase synchronous machine with and without damper bars and 3-phase induction machine, Kron’s primitive Machine-voltage, current and Torque equations.

UNIT II: DC MACHINE MODELING:
Mathematical model of separately excited D.C motor – Steady State analysis-Transient State analysis-Sudden application of Inertia Load-Transfer function of Separately excited D.C Motor- Mathematical model of D.C Series motor, Shunt motor-Linearization Techniques for small perturbations

UNIT III: MODELING OF THREE PHASE INDUCTION MACHINE – I:
Transformation from Three phase to two phase and Vice Versa - Transformation from Rotating axes to stationary axes and vice versa –Park’s Transformation and it’s physical concept –The Inductance matrix-Mathematical model of Induction machine –Steady State analysis.

UNIT IV: MODELING OF THREE PHASE INDUCTION MACHINE – II:

UNIT V: MODELING OF SINGLE PHASE INDUCTION MACHINE:
Comparison between single phase and poly-phase induction motor - Cross field theory of single-phase induction machine, steady state analysis – steady state torque

UNIT VI: MODELING OF SYNCHRONOUS MACHINE:
Synchronous machine inductances –The phase Co-ordinate model-The Space phasor (d-q) model-Steady state operation-Mathematical model of PM Synchronous motor.

UNIT VII: MODELING OF SPECIAL MACHINES –I:
Modelling of Permanent Magnet Brushless DC Motor – Operating principle-Mathematical modeling of PM Brushless DC motor-PMDC Motor Drive Scheme.

UNIT VIII: MODELING OF SPECIAL MACHINES –II:

TEXT BOOKS:
REFERENCE BOOKS:

2. Electrical Drives- I. Boldea & S.A. Nasar-The Oxford Press Ltd.
4. Electromechanical Dynamics- Woodson & Melcher-John Wiley & Sons
UNIT I: INTRODUCTION TO DIGITAL SIGNAL PROCESSING


UNIT II: DIGITAL FILTER STRUCTURES

Block Diagram representation, Equivalent structures, Basic FIR Digital Filter structures, Basic IIR Digital Filter structures, Realization of Basic structures using MATLAB, All pass filters, Computational complexity of Digital filter structures.

UNIT III: IIR DIGITAL FILTER DESIGN

Preliminary considerations, Bilinear transformation method of IIR Filter design, Design of low pass IIR Digital filters, Design of High pass, Band pass and band stop IIR digital filters, Spectral Transformations of IIR filter.

UNIT IV: FIR DIGITAL FILTER DESIGN

Preliminary considerations, FIR filter design based on windowed Fourier series, Computer aided design of Equiripple Linear phase FIR filters, Design of Minimum phase FIR filters. Design of computationally efficient FIR digital filters.

UNIT V: FINITE WORD LENGTH EFFECTS

Introduction- Effects of coefficients on Quantization- Quantization in sampling analog signals- Finite register length effects in realization of Digital Filters- Discrete Fourier transform computations

UNIT VI: ARCHITECTURE OF TMS320LF 2407A

Introduction – Architectural overview – Memory and I/O spaces - Internal architecture – Central Processing Unit (CPU) – Program control.

UNIT VII: ADDRESSING MODES AND ASSEMBLY LANGUAGE INSTRUCTIONS OF C2XXX & PERIPHERALS (THE EVENT MANAGERS)

Data formats – Addressing modes – groups of addressing mode – Assembly language instructions - Event Manager (EV) Functional Blocks- Event Manager (EV) Register Addresses- General-Purpose (GP) Timers - Compare Units- PWM Circuits Associated with Compare Units- PWM Waveform Generation with Compare Units and PWM Circuits-Space Vector PWM- Capture Units- Quadrature Encoder Pulse (QEP) Circuit - Event Manager (EV) Interrupts

UNIT VIII: APPLICATIONS IN DSP CONTROLLER

Applications – DSP controlled DC motor drives – DSP controlled AC motor drives- Different types of PWM Techniques using DSP-Model for converter and inverter- 6 pulse and 24 pulse controllers for cycloconverter - Comparison of FPGA controller with DSP controller.

TEXT BOOKS:


REFERENCES:


3. TMS320F/C24x DSP Controllers-Reference Guide-CPU and Instruction Set

UNIT I SAMPLING AND RECONSTRUCTION
Introduction to Digital Control Systems, Quantization and Quantization error – Introduction, Examples of Data control systems – Digital to Analog conversion and Analog to Digital conversion, sample and hold operations.

UNIT II THE Z – TRANSFORMS
Introduction, Linear difference equations, pulse response, Z – transforms, Theorems of Z – Transforms, the inverse Z – transforms, Modified Z- Transforms

UNIT III Z-PLANE ANALYSIS OF DISCRETE-TIME CONTROL SYSTEM
Z-Transform method for solving difference equations; Pulse transforms function, block diagram analysis of sampled – data systems, mapping between s-plane and z-plane.

UNIT IV STATE SPACE ANALYSIS
State Space Representation of discrete time systems, Pulse Transfer Function Matrix solving discrete time state space equations, State transition matrix and it’s Properties, Methods for Computation of State Transition Matrix, Discretization of continuous time state – space equations

UNIT V CONTROLLABILITY AND OBSERVABILITY
Concepts of Controllability and Observability, Tests for controllability and Observability. Duality between Controllability and Observability, Controllability and Observability conditions for Pulse Transfer Function

UNIT VI STABILITY ANALYSIS

UNIT VII DESIGN OF DISCRETE TIME CONTROL SYSTEM BY CONVENTIONAL METHODS

UNIT VIII STATE FEEDBACK CONTROLLERS AND OBSERVERS
Design of state feedback controller through pole placement – Necessary and sufficient conditions, Ackerman’s formula.State Observers – Full order and Reduced order observers.

TEXT BOOKS:

REFERENCE BOOKS:
2. Digital Control and State Variable Methods by M.Gopal, TMH
UNIT I: INTRODUCTION
Conventional design procedures – Limitations – Need for field analysis based design.

UNIT II: MATHEMATICAL FORMULATION OF FIELD PROBLEMS

UNIT III: LAPLACE AND POISSON’S EQUATIONS

UNIT IV: PHILOSOPHY OF FEM -I

UNIT V: PHILOSOPHY OF FEM-II

UNIT VI: CAD PACKAGES
Elements of CAD System – Pre-processing – Modelling – Meshing Material properties - Boundary Conditions– Setting up solution – Post processing.

UNIT VII: DESIGN APPLICATIONS -I
Design of Solenoid Actuator – Induction Motor

UNIT VIII: DESIGN APPLICATIONS -II
Insulators – Power transformer.

TEXT BOOKS:

REFERENCE BOOKS:
UNIT I: 8051 MICROCONTROLLERS

Introduction to Intel 8 bit & 16 bit Microcontrollers, MCS-51 Architecture, Registers in MCS-51, 8051 Pin Description, 8051 Connections, 8051 Parallel I/O Ports, Memory Organization

UNIT II: MCS-51 ADDRESSING MODES AND INSTRUCTIONS

8051 Addressing Modes, MCS-51 Instruction Set, 8051 Instructions and Simple Programs, Using Stack Pointer, 8051 Assembly Language Programming, Development Systems and Tools, Software Simulators of 8051

UNIT III: MCS-51 INTERRUPTS, TIMER/COUNTERS AND SERIAL COMMUNICATION

Interrupts, Interrupts in MCS-51, Timers and Counters, Serial Communication, Atmel Microcontrollers (89CXX and 89C20XX), Architectural Overview of Atmel 89C51 and Atmel 89C2051, Pin Description of 89C51 and 89C2051, Using Flash Memory Devices Atmel 89CXX and 89C20XX

UNIT IV: APPLICATIONS OF MCS-51 AND ATMEL 89C51 AND 89C2051 MICROCONTROLLERS

Applications of MCS-51 and Atmel 89C51 and 89C2051 Microcontrollers- Square Wave Generation- Rectangular Waves- Pulse Generation- Pulse Width Modulation- Staircase Ramp Generation- Sine Wave Generation- Pulse Width Measurement- Frequency Counter

UNIT V: PIC MICROCONTROLLERS

PIC Microcontrollers: Overview and Features, PIC 16C6X/7X, FSR(File Selection Register) [Indirect Data Memory Address Pointer], PIC Reset Actions, PIC Oscillator Connections, PIC Memory Organizations, PIC 16C6X/7X Instructions, Addressing Modes, I/O Ports, Interrupts in PIC 16C61/71, PIC 16C61/71 Timers, PIC 16C71 Analog-to-Digital Converter (ADC)

UNIT VI: PIC 16F8XX FLASH MICROCONTROLLERS

Introduction, Pin Diagram of 16F8XX, STATUS Register, OPTION_REG Register, Power Control Register (PCON), PIC 16F8XX Program Memory, PIC 16F8XX Data Memory, DATA EEPROM and Flash Program EEPROM, Interrupts in 16F877, I/O Ports, Timers

UNIT VII: INTERFACING AND MICROCONTROLLER APPLICATIONS-

Light Emitting Diodes (LEDs), Push Buttons, Relays and Latch Connections, Keyboard Interfacing, Interfacing 7-Segment Displays, LCD Interfacing, ADC AND DAC Interfacing with 89C51 Microcontrollers.

UNIT VIII: INDUSTRIAL APPLICATIONS OF MICROCONTROLLERS

Measurement Applications, Automation and Control Applications

TEXT BOOKS:


Reference books:

1. Microcontrollers by Kennith Jayala, Thomson publishers
2. Microprocessor and Microcontrollers by Prof C.R.Sarma
UNIT I : INTRODUCTION :

UNIT II : ADVANCED TECHNIQUES IN SIMULATION –I :
Analysis of power electronic systems in a sequential manner – coupled and decoupled systems

UNIT III : ADVANCED TECHNIQUES IN SIMULATION–II :
Various algorithms for computing steady state solution in power electronic systems – Future trends in computer simulation.

UNIT IV : MODELING OF POWER ELECTRONIC DEVICES :

UNIT V : SIMULATION OF CIRCUITS – I :
Introduction – Schematic capture and libraries – Time domain analysis – System level integration and analysis –

UNIT VI : SIMULATION OF CIRCUITS– I :

UNIT VII : CASE STUDIES–I:
Simulation of Converters, Choppers, Inverters, AC voltage controllers, and Cycloconverters feeding R, R-L, and R-L-E loads

UNIT VII : CASE STUDIES–I:
Computation of performance parameters: harmonics, power factor, angle of overlap.

TEXT BOOKS :

REFERENCES :
UNIT I: ECONOMIC OPERATION OF POWER SYSTEM


UNIT II: UNIT COMMITMENT PROBLEM

Introduction to UCP, thermal & Hydel constraints in Unit commitment: Priority list scheme method, unit commitment problem solution by priority list scheme method. Unit commitment problem solution by Dynamic programming Approach. Introduction, advantages of DP method over priority list scheme, forward DP approach and their flow charts solution UCP using Dynamic program method.

UNIT III: LOAD FREQUENCY CONTROL

Necessity of keeping frequency constant. Definition of control area, single area control, Block diagram representation of an isolated power system, steady state analysis, and Dynamic response-Uncontrolled case. Load frequency control of 2-area system: uncontrolled case and controlled case. Tie-line bias control

UNIT IV: PROPORTIONAL PLUS INTEGRAL CONTROL

Proportional plus integral control of single area and its block diagram representation, steady state response, load frequency control and Economic dispatch control. Optimal LF control-steady state representation, performance index and optimal parameter adjustment

UNIT V: INTERCHANGE OF POWER BETWEEN INTER CONNECTED SYSTEM


UNIT VI: POWER SYSTEM SECURITY & CONTINGENCY ANALYSIS


UNIT VII: REACTIVE POWER – VOLTAGE CONTROL

Reactive power control, excitation systems – modelling, static and dynamic analysis, stability compensation, generation and absorption of reactive power, relation between voltage, power and reactive power at a node, method of voltage control, tap changing transformers, tap setting of OLTC transformer and MVAR injection of switched capacitors.

UNIT VIII: COMPUTER CONTROL OF POWER SYSTEMS

Need of computer control of power systems, concept of energy control center (or) load dispatch center and the functions, system monitoring, data acquisition and control, system hardware configuration, SCADA and EMS functions, network topology, state estimation, security analysis and control, operating states.
TEXTBOOKS:

REFERENCE:
SIMULATION OF POWER ELECTRONIC SYSTEMS LAB

LIST OF EXPERIMENTS

1. PSPICE simulation of single phase Semi & full converter using R-L-E load
2. PSPICE simulation of single phase AC voltage controller using R-L-E load
3. PSPICE simulation of Three phase Semi & Full converter using R-L-E load
4. PSPICE simulation of single phase inverter with Two Level PWM control
5. PSPICE simulation of single phase inverter with Three Level PWM control
6. PSPICE simulation of Buck, Boost & Buck-Boost Converters
7. Simulation of Open Loop Control of PMSM Using MATLAB Simulink
8. Simulation of speed control of separately excited DC Motor using MATLAB Simulink
9. Simulation of induction motor with indirect vector control using MATLAB Simulink
10. Simulation of induction motor with Closed loop constant V/F control using MATLAB Simulink
I M.Tech –I Semester (PE & ED) (12BPE12) D.C DRIVES LAB

LIST OF EXPERIMENTS

1. Single phase half wave controlled converter with resistive-inductive load
2. Single phase fully controlled converter with resistive-inductive load
3. Thyristorised drive for PMDC motor with speed measurement & closed loop control
4. Speed measurement of PMDC motor with closed loop control
5. IGBT using single 4 quadrant chopper drive for PMDC motor with speed measurement and closed loop and control
6. Thyristorised drive for dc motor with closed loop control
7. Three phase input thyristorised drive 3hp dc motor with closed loop control
8. Three phase input IGBT drive for 4 quadrant chopper of 3HP dc motor with closed loop control
9. Operation of 3-phase Full-Converter on R & R-L load
10. Performance & speed control of D.C. drive using 3-phase full Converter
(12BPE13) SEMINAR-I
UNIT I: PULSE WIDTH MODULATED INVERTERS (SINGLE PHASE INVERTER):

Introduction-Principle of operation – Performance parameters- Single phase half bridge inverter-evaluation of output voltage and current with resistive, inductive and capacitive loads Voltage control of single phase inverters Single PWM-Multiple PWM-Sinusoidal PWM-modified PWM-phase displacement control – numerical problems

UNIT II: ADVANCED MODULATION TECHNIQUES (SINGLE PHASE INVERTER):

Advanced Modulation techniques for improved performance, Trapezoidal, staircase, stepped, harmonic injection and delta modulation – Advantage - Application- numerical problems

UNIT III: PULSE WIDTH MODULATED INVERTERS (THREE PHASE INVERTER):

Three Phase inverters-analysis of 180 degree condition of output voltage and current with resistive, inductive loads-analysis of 120 degree conduction-Voltage control of three phase inverters-sinusoidal PWM-third harmonic PWM-60 degree PWM – comparison of PWM techniques - numerical problems

UNIT IV: SPACE VECTOR MODULATION:

Space vector modulation-Comparison of PWM techniques-harmonic reduction – current source inverters-Variable dc link inverter -boost inverters- buck and boost inverter – inverter circuit design – Advantage--Application- numerical problems

UNIT V: HARMONIC REDUCTIONS:

Third harmonic PWM-60 degree PWM- Phase displacement-Bipolar output voltage notches Uni-polar output voltage notches-Transformer connections-Design of C filter to eliminate harmonics- numerical problems

UNIT VI: CURRENT SOURCE INVERTER:


UNIT VII: MULTILEVEL INVERTER:

Multilevel concept – Diode clamped – Flying capacitor – Cascade type multilevel Inverters - Comparison of multilevel Inverters - Application of multilevel Inverters

UNIT VIII: RESONANT INVERTERS:


TEXT BOOKS:

REFERENCE BOOKS:
UNIT I: INTRODUCTION TO AC DRIVES:

Introduction to motor drives-torque production- Equivalent circuit analysis-Speed-Torque characteristics with variable voltage operation, variable frequency operation, constant v/f operation-Induction motor characteristics in constant torque and field weakening regions

UNIT II: CONTROL OF INDUCTION MOTOR DRIVES AT STATOR SIDE:

Scalar control-Voltage fed inverter control-Open loop volts/Hz Control-Speed control-Torque control with torque and flux control-Independent current and frequency control-Speed and flux control in current fed inverter drive-Volts/Hertz Control current fed-Inverter drive-Efficiency optimization control by flux program

UNIT III: CONTROL OF INDUCTION MOTOR AT ROTOR SIDE:

Slip power recovery drives-Static Kramer Drive-Phasor diagram-Torque expression-Speed control of Kramer Drive-Static Scheribus Drive- Modes of operation

UNIT IV: VECTOR CONTROL OF INDUCTION MOTOR DRIVES:

Principles of Vector Control-Vector Control Methods-Direct method of Vector control-Adaptive control principles-Self tuning regulator-Model referencing control

UNIT V: CONTROL OF SYNCHRONOUS MOTOR DRIVES:

Synchronous motor and its characteristics - control strategies - constant torque angle control-Unity power factor control-Constant mutual flux linkage control

UNIT VI: CONTROLLERS:

Flux weakening operation- Maximum speed-Direct flux weakening algorithm - Constant torque mode controller- Flux Weakening controller- Indirect flux weakening – Maximum permissible torque-Speed control scheme- Implementation strategy – Speed controller design

UNIT VII: VARIABLE RELUCTANCE MOTOR DRIVE:

Variable reluctance motor drives- Torque Production in the variable reluctance motor- Drive characteristics and control principles- Current control variable reluctance servo drive.

UNIT VIII: BRUSHLESS DC MOTOR DRIVES:

Three phase full wave Brushless dc motor – Sinusoidal type of Brushless dc motor-Current controlled Brushless dc servo drives

TEXT BOOKS:

REFERENCES:

1. Power Electronic Control of AC motors- MD Murphy & FG Turn Bull Pergman Press(For Chapters II,III, V) – 1st Edition
2. Power Electronics Circuits , Devices and Application- M.H Rashid –PHI 1995
UNIT I: INTRODUCTION

Environmental aspects of electric energy conversion: impacts of renewable energy generation on environment (cost-GHG Emission)

UNIT II: QUALITATIVE STUDY OF DIFFERENT RENEWABLE ENERGY RESOURCES:

Qualitative study of different renewable energy resources: Solar, wind, ocean, Biomass, Fuel cell, Hydrogen energy systems and hybrid renewable energy systems.

UNIT III: ELECTRICAL MACHINES FOR RENEWABLE ENERGY CONVERSION

Review of reference theory fundamentals-principle of operation and analysis: IG, PMSG, SCIG and DFIG.

UNIT IV: POWER CONVERTERS

Solar: Block diagram of solar photo voltaic system -Principle of operation: line commutated converters (inversion-mode) - Boost and buck-boost converters- selection of inverter, battery sizing, and array sizing Wind

UNIT V: THREE PHASE AC VOLTAGE CONTROLLERS

AC-DC-AC converters: uncontrolled rectifiers, PWM Inverters, Grid Interactive Inverters-matrix converters.

UNIT VI: ANALYSIS OF WIND AND PV SYSTEMS

Stand alone operation of fixed and variable speed wind energy conversion systems and solar system

UNIT VII: GRID CONNECTION ISSUES

Grid integrated PMSG and SCIG Based WECS Grid Integrated solar system

UNIT VIII: HYBRID RENEWABLE ENERGY SYSTEMS

Need for Hybrid Systems- Range and type of Hybrid systems- Case studies of Wind-PV Maximum Power Point Tracking (MPPT).

TEXT BOOKS:


REFERENCES:

UNIT I LOAD COMPENSATION IN POWER SYSTEMS:


UNIT II UNCOMPENSATED TRANSMISSION LINES:

Uncompensated electrical parameters-Transmission line equation-Solution of transmission line wave equation-Surge impedance and natural loading –Uncompensated on open circuit-voltage and current profile-Uncompensated under load conditions-Maximum and stability consideration-effect of generator reactance.

UNIT III STATIC COMPENSATION CONTROL:


UNIT IV COMMUTATION METHODS FOR CONTROLLED CONVERTERS:

Methods of employing natural commutation – Methods of employing forced commutation and implementation of forced commutation.

UNIT V HARMONICS CONTROL & POWER FACTOR IMPROVEMENT:

Reactive Power Variation for Fully Controlled Converter – Half Controlled Converter – Fully Controlled Converter with controlled freewheeling.

UNIT VI VOLTAGE REGULATORS:

Introduction to voltage regulators – Manually Controlled voltage regulator (Conventional methods). Static tap changer using Thyristors – Different control schemes and comparison.

UNIT VII SWITCH MODE POWER SUPPLY (SMPS):

Introduction to Switch Mode Power Supply (SMPS) – Parallel UPS – Redundant UPS – Non-redundant UPS – UPS using resonant power converters.

UNIT VIII HIGH VOLTAGE DC TRANSMISSION:

Analysis of HVDC Converters : Pulse number – Choice of converter configuration – Simplified analysis of graetz circuit – Converter bridge characteristics.

Converted and HVDC system control : Principles of DC link control – Converter control characteristics – System control hierarchy – firing control – current and extinction angle control – starting and stopping of DC link power control.

TEXT BOOKS:

REFERENCE BOOKS:

SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY  
(AUTONOMOUS)  
R.V.S. NAGAR, TIRUPATI ROAD, CHITTOOR-517127. A.P  
DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING  

I M.Tech –II Semester (PE & ED)  

(ELECTIVE-III)  
(12BPE18) EMBEDDED SYSTEM DESIGN  

UNIT I : THE 8051 MICROCONTROLLERS :  
Embedded system concepts – Embedded Hardware devices – Introduction to 8051 microcontroller – 8051 Derivatives  

UNIT II: THE 8051 MICROCONTROLLERS ARCHITECTURE:  
Architecture of 8051 microcontroller - Memory Organization - Addressing Modes - Assembly Language Instructions.  

UNIT III: EMBEDDED SYSTEM PROGRAMMING:  
Embedded Software Tools - Assembler - Compiler - Simulator - Debugger – In circuit Simulator – Integrator Development Environment (IDE) - Introduction to Embedded ‘C’ Programming - Programming in Embedded Controllers.  

UNIT IV: EMBEDDED PERIPHERALS & INTERFACING:  
Embedded Peripherals - General Purpose I/O - Timer - Counter - UART/USART-Interrupts - ADC-DAC – Parallel Port - Peripheral Interfacing with input/output devices - LED-LCD – Keyboard - ADC - DAC.  

UNIT V: RISC EMBEDDED CONTROLLERS:  
Comparison of CISC and RISC Controllers - Pipelining Architecture - Introduction to PIC Microcontrollers  

UNIT VI: RISC EMBEDDED CONTROLLERS:  

UNIT VII: DISTRIBUTED EMBEDDED SYSTEM DESIGN:  
Distributed Embedded System – Embedded Networking - RS232-RS485 - Inter-Integrated Circuit (I2 C) – Serial Peripheral Interface (SPI) –  

UNIT VIII: DISTRIBUTED EMBEDDED SYSTEM DESIGN:  
Universal Serial Bus (USB) - Controller Area Network (CAN) - Embedded Networking using Ethernet devices.  

TEXT BOOKS:  
REFERENCES:  
1. Myke Predko, "Programming & Customizing PIC Microcontrollers".  
2. Zdravko Karakehayov, "Embedded System Design with 8051 Microcontrollers".  
WEBSITES:  
1. www.raisonance.com  
2. www.ccsinfo.com  
3. www.micrchip.com  
4. www.atmel.com  

Department of Electrical and Electronics Engineering  

Page 40
UNIT I : INTRODUCTION


UNIT II : ARTIFICIAL NEURAL NETWORKS – I :

Concept of Artificial Neural Networks and its basic mathematical model, McCulloch - Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron. Learning and Training the neural network.

UNIT III : ARTIFICIAL NEURAL NETWORKS I :

Principal - Component analysis and wavelet transformations. Hopfield network, Self - Organizing network and Recurrent network. Design of logic using all algorithms. Neural Network based controller with any application.

UNIT IV : GENETIC ALGORITHM :

Concept of Genetic algorithm and detail algorithmic steps, Genetic operators - Solution of typical control problems using genetic algorithm-Concept on some other search techniques like tabu search and ant-colony search techniques for solving optimization problems.

UNIT V : FUZZY LOGIC SYSTEM :

Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning. Introduction to fuzzy logic modeling and control. Fuzzification, inferencing

UNIT VI : FUZZY LOGIC SYSTEM :

Defuzzification. Fuzzy knowledge and rule bases. Fuzzy modeling and control schemes for nonlinear systems. Self-organizing fuzzy logic control.

UNIT VII : APPLICATION :


UNIT VIII : FUZZY LOGIC & NEURAL NETWORK APPLICATIONS TO DRIVES


Neural network applications:-PWM Controller-Selected harmonic elimination PWM-Space vector PWM-Vector controlled drive-feedback signal estimation-speed estimation and flux estimation of induction motor
TEXT BOOKS:

REFERENCE BOOKS:
UNIT I: POWER SYSTEM HARMONICS & LINE COMMUTATED RECTIFIERS

Average power-RMS value of a waveform-Power factor-AC line current harmonic standards IEC 1000-IEEE 519- The Single phase full wave rectifier-Continuous Conduction Mode-Discontinuous Conduction Mode-Behaviour when C is large

UNIT II: MINIMIZING THD

Minimizing THD when C is small-Three phase rectifiers- Continuous Conduction Mode- Discontinuous Conduction Mode-Harmonic trap filters.

UNIT III: PULSE WIDTH MODULATED RECTIFIERS

Properties of Ideal rectifiers-Realization of non ideal rectifier-Control of current waveform-Average current control-Current programmed Control- Hysteresis control-Nonlinear carrier control

UNIT IV: SINGLE PHASE CONVERTER SYSTEM

Single phase converter system incorporating ideal rectifiers- Modeling losses and efficiency in CCM high quality rectifiers-Boost rectifier Example - expression for controller duty cycle-expression for DC load current-solution for converter Efficiency S.

UNIT V: RESONANT CONVERTERS


UNIT VI: ZERO CURRENT SWITCHING


UNIT VII: DYNAMIC ANALYSIS OF SWITCHING CONVERTERS

Review of linear system analysis-State Space Averaging-Basic State Space Average Model-State Space Averaged model for an ideal Buck Converter, ideal Boost Converter, ideal Buck Boost Converter, for an ideal Cuk Converter.

UNIT VIII: CONTROL OF RESONANT CONVERTERS

Pulse Width Modulation-Voltage Mode PWM Scheme-Current Mode PWM Scheme-Design of Controllers: PI Controller, Variable Structure Controller, Optimal Controller for the source current shaping of PWM rectifiers.

TEXT BOOKS:


REFERENCES

1. William Shepherd and Li zhang “Power Converters Circuits” Marceld Ekkerin, C.
2. Simon Ang and Alejandro Oliva “Power- Switching Converters” Taylor & Francis Group
UNIT I: INTRODUCTION

UNIT II: THE CALCULUS OF VARIATIONS – I

UNIT III: THE CALCULUS OF VARIATIONS - II

UNIT IV: VARIATIONAL APPROACH TO OPTIMAL

UNIT V: NUMERICAL DETERMINATION OF OPTIMAL TRAJECTORIES
Two-Point Boundary-Value Problem- Method of Steepest Descent –Steepest Descent Algorithm.

UNIT VI: PONTRYAGIN’S MINIMUM PRINCIPLE

UNIT VII: DYNAMIC PROGRAMMING-I

UNIT VIII: DYNAMIC PROGRAMMING-II

TEXT BOOKS:
1. Optimal Control Theory- Donald E. Krik

REFERENCES:
2. Modern Control Systems Theory- M.Gopal
UNIT I: MODELS FOR IDENTIFICATION
Models of LTI systems: Linear Models-State space Models-OE model- Model sets, Structures and Identifiability

UNIT II: MODELS FOR TIME-VARYING AND NON-LINEAR SYSTEMS:
Models with Nonlinearities – Non-linear state-space models-Black box models, Fuzzy models’.

UNIT III: NON-PARAMETRIC AND PARAMETRIC IDENTIFICATION

UNIT IV: NON-LINEAR IDENTIFICATION AND MODEL VALIDATION
Open and closed loop identification: Approaches – Direct and indirect identification – Joint input-output identification – Non-linear system identification

UNIT V: WIENER MODELS
Power series expansions - State estimation techniques – Non linear identification using Neural Network and Fuzzy Logic.

UNIT VI: ADAPTIVE CONTROL AND ADAPTATION TECHNIQUES
Introduction – Uses – Auto tuning – Self Tuning Regulators (STR) – Model Reference Adaptive Control (MRAC) – Types of STR and MRAC

UNIT VII: DIFFERENT APPROACHES TO SELF TUNING REGULATORS
Different Approaches to Self Tuning Regulators- Stochastic Adaptive control – Gain Scheduling.

UNIT VIII: CASE STUDIES
Inverted Pendulum, Robot arm, process control application: heat exchanger, Distillation column, application to power system, Ship steering control.

TEXT BOOKS:
2. Torsten Soderstrom, Petre Stoica, “System Identification”, prentice Hall ‘

REFERENCES:
1. Astrom and Wittenmark,” Adaptive Control “, PHI
2. William S. Levine, ” Control Hand Book”.
UNIT I:

General: Introduction to Distribution systems, an overview of the role of computers in distribution system planning-Load modeling and characteristics: definition of basic terms like demand factor, utilization factor, load factor, plant factor, diversity factor, coincidence factor, contribution factor and loss factor - Relationship between the load factor and loss factor - Classification of loads (Residential, Commercial, Agricultural and Industrial) and their characteristics.

UNIT II:

Distribution Feeders and Substations: Design consideration of Distribution feeders: Radial and loop types of primary feeders, voltage levels, feeder-loading.

UNIT III:

Design practice of the secondary distribution system. Location of Substations: Rating of a Distribution Substation, service area with primary feeders. Benefits derived through optimal location of substations.

UNIT IV:

System analysis: Voltage drop and power loss calculations: Derivation for volt-drop and power loss in lines, manual methods of solution for radial networks, three-phase balanced primary lines, non-three-phase primary lines.

UNIT V:

Protective devices and coordination: Objectives of distribution system protection, types of common faults and procedure for fault calculation.

UNIT VI:


UNIT VII:

Capacitive compensation for power factor control: Different types of power capacitors, shunt and series capacitors, effect of shunt capacitors (Fixed and switched) power factor correction, capacitor location. Economic justification. Procedure to determine the best capacitor location.

UNIT VIII:

Voltage control: Equipment for voltage control, effect of series capacitors, effect of AVB/AVR, line drop compensation.

TEXT BOOKS:


REFERENCE BOOKS:

LIST OF EXPERIMENTS

1. Performance & speed control of 3 phase slip ring Induction motor by Static Rotor Resistance controller
2. Single phase cyclo converter based ac induction motor controller
4. Single phase half wave controlled AC voltage controller with resistive-inductive load
5. Single phase fully controlled AC voltage controller with resistive-inductive load
6. Single Phase IGBT based PWM Inverter on R & R-L load
7. Operation of 3-phase IGBT based PWM Inverter on R & R-L load
8. Three phase PWM Pulse generation using PIC Micro controller
9. PIC Microcontroller based speed control of three phase Induction Motor
10. DSP based V/F Control of 3 phase Induction motor
LIST OF EXPERIMENTS

1. a. Arithmetic operations manipulation for 8051
   b. Arithmetic operations with the stack for 8051.
2. a. Direct Bank Addressing.
   b. Indirect Addressing.
3. Accessing Scratchpad RAM
4. Creating Variable Arrays
5. State Machines
6. Interfacing of Button and LED to 89C51.
7. Interfacing of an Electro Mechanical Relay.
8. Interfacing of Stepper Motor to 89C51
9. Study on PWM generation using Timer 1, 2, 3.
10. Study of six pulse PWM generation using full compare unit with dead band timer
SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY (AUTONOMOUS)
R.V.S. NAGAR, TIRUPATI ROAD, CHITTOOR-517127. A.P
DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

I M.Tech –II Semester (PE & ED)

L  T  P  C
2

(12BPE26) SEMINAR- II

SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY (AUTONOMOUS)
R.V.S. NAGAR, TIRUPATI ROAD, CHITTOOR-517127. A.P
DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

I M.Tech –II Semester (PE & ED)

L  T  P  C
2

(12BPE27) COMPREHENSIVE VIVA VOCE

SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY (AUTONOMOUS)
R.V.S. NAGAR, TIRUPATI ROAD, CHITTOOR-517127. A.P
DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

I M.Tech –III & IV Semester (PE & ED)

L  T  P  C
16

(12BPE28) PROJECT WORK